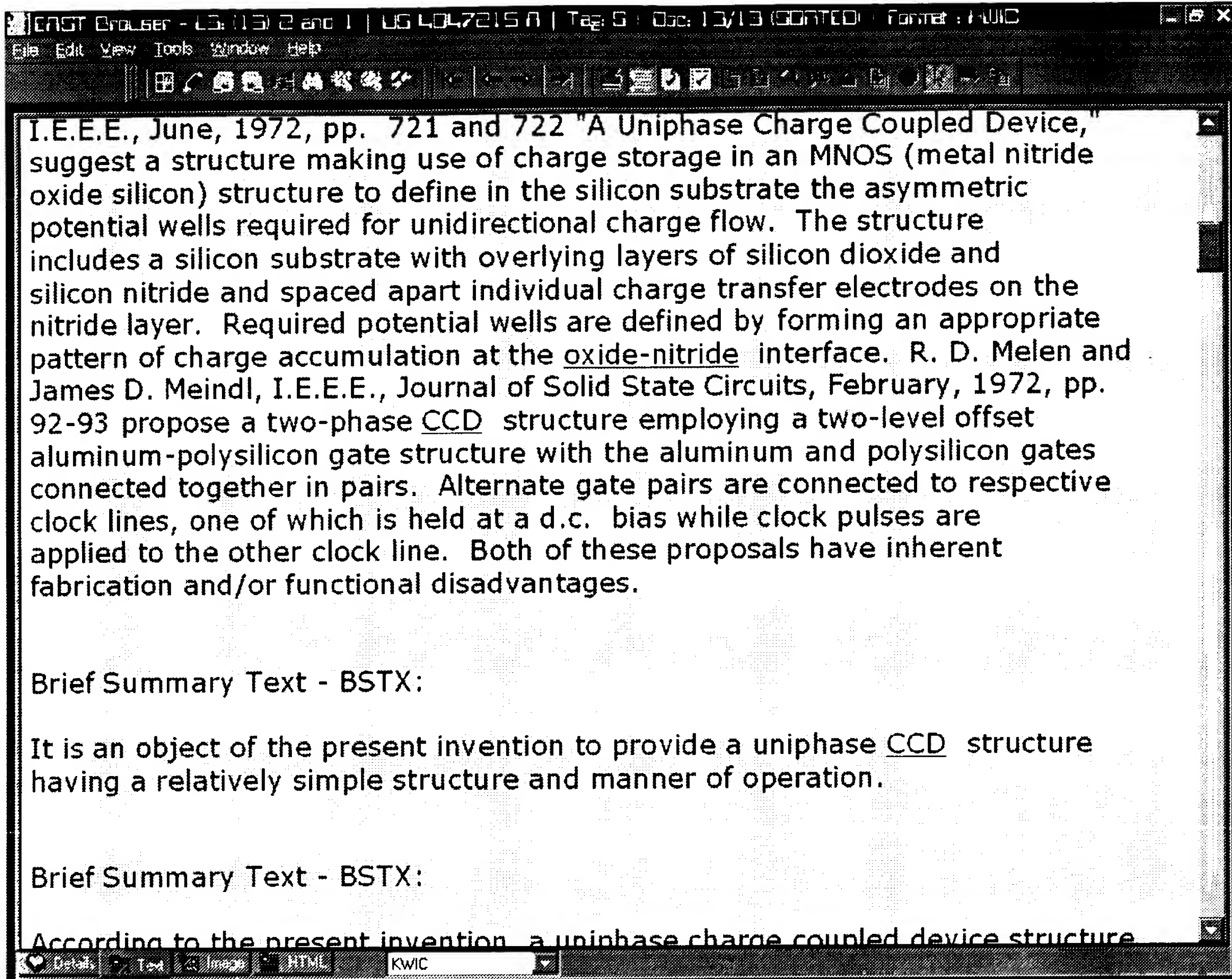


L Number	Hits	Search Text	DB	Time stamp
1	42385	ccd	USPAT; US-PGPUB	2002/07/29 07:47
2	408	"oxide-nitride"	USPAT; US-PGPUB	2002/07/29 07:48
3	13	"oxide-nitride" and ccd	USPAT; US-PGPUB	2002/07/29 07:58
4	5171	"gate dielectric"	USPAT; US-PGPUB	2002/07/29 07:59
5	23569	oxide near2 nitride	USPAT; US-PGPUB	2002/07/29 07:59
6	289	"gate dielectric" with (oxide near2 nitride)	USPAT; US-PGPUB	2002/07/29 07:59
7	0	ccd with ("gate dielectric" with (oxide near2 nitride))	USPAT; US-PGPUB	2002/07/29 08:00
8	123	ccd and "gate dielectric"	USPAT; US-PGPUB	2002/07/29 08:00
9	84272	nitride	USPAT; US-PGPUB	2002/07/29 08:00
10	71	(ccd and "gate dielectric") and nitride	USPAT; US-PGPUB	2002/07/29 08:00
11	201472	@ad>20000626 or @rlad>20000626	USPAT; US-PGPUB	2002/07/29 08:01
12	65	((ccd and "gate dielectric") and nitride) not (@ad>20000626 or @rlad>20000626)	USPAT; US-PGPUB	2002/07/29 08:01



I.E.E.E., June, 1972, pp. 721 and 722 "A Uniphase Charge Coupled Device," suggest a structure making use of charge storage in an MNOS (metal nitride oxide silicon) structure to define in the silicon substrate the asymmetric potential wells required for unidirectional charge flow. The structure includes a silicon substrate with overlying layers of silicon dioxide and silicon nitride and spaced apart individual charge transfer electrodes on the nitride layer. Required potential wells are defined by forming an appropriate pattern of charge accumulation at the oxide-nitride interface. R. D. Melen and James D. Meindl, I.E.E.E., Journal of Solid State Circuits, February, 1972, pp. 92-93 propose a two-phase CCD structure employing a two-level offset aluminum-polysilicon gate structure with the aluminum and polysilicon gates connected together in pairs. Alternate gate pairs are connected to respective clock lines, one of which is held at a d.c. bias while clock pulses are applied to the other clock line. Both of these proposals have inherent fabrication and/or functional disadvantages.

Brief Summary Text - BSTX:

It is an object of the present invention to provide a uniphase CCD structure having a relatively simple structure and manner of operation.

Brief Summary Text - BSTX:

According to the present invention a uniphase charge coupled device structure

There have previously been reported proposals for CCDs using only a single clock signal. P. P. Gelberger and C. A. T. Salama, Proceedings of the I.E.E.E., June, 1972, pp. 721 and 722 "A Uniphase Charge Coupled Device," suggest a structure making use of charge storage in an MNOS (metal nitride oxide silicon) structure to define in the silicon substrate the asymmetric potential wells required for unidirectional charge flow. The structure includes a silicon substrate with overlying layers of silicon dioxide and silicon nitride and spaced apart individual charge transfer electrodes on the nitride layer. Required potential wells are defined by forming an appropriate pattern of charge accumulation at the oxide-nitride interface. R. D. Melen and James D. Meindl, I.E.E.E., Journal of Solid State Circuits, February, 1972, pp. 92-93 propose a two-phase CCD structure employing a two-level offset aluminum-polysilicon gate structure with the aluminum and polysilicon gates connected together in pairs. Alternate gate pairs are connected to respective clock lines, one of which is held at a d.c. bias while clock pulses are applied to the other clock line. Both of these proposals have inherent fabrication and/or functional disadvantages.

#### Brief Summary Text - BSTX:

It is an object of the present invention to provide a uniphase CCD structure having a relatively simple structure and manner of operation.



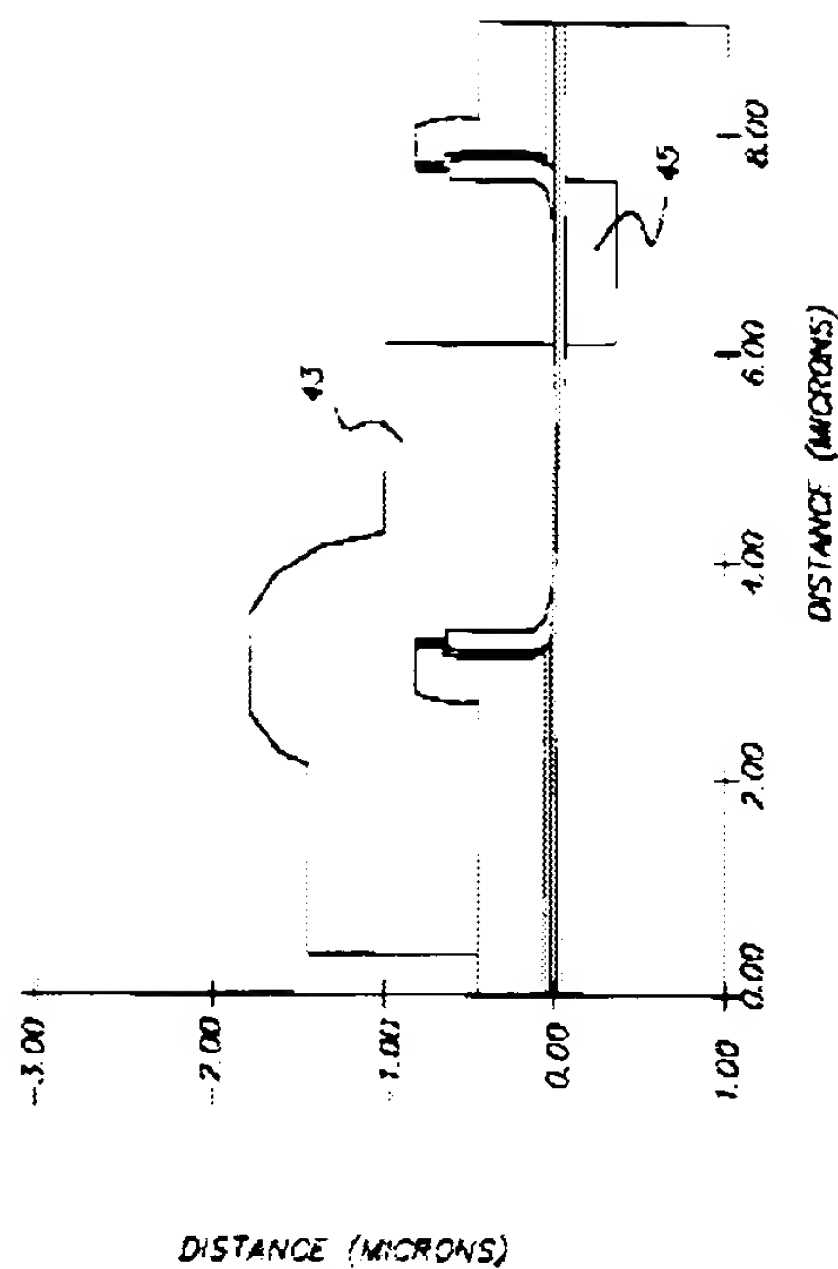


FIG. 2g



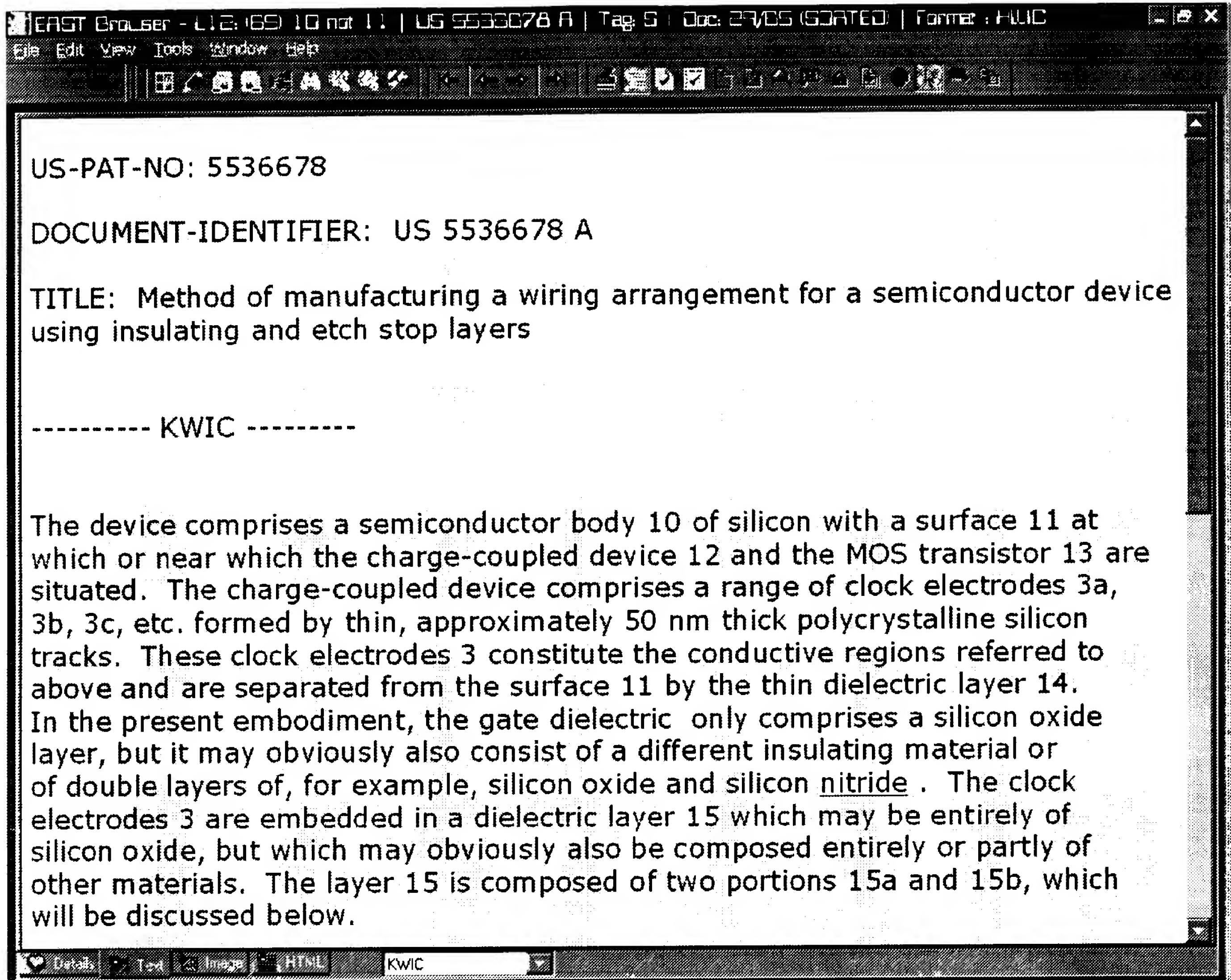
US-PAT-NO: 6051852

DOCUMENT-IDENTIFIER: US 6051852 A

TITLE: Self aligned LOD antiblooming structure for solid-state imagers

----- KWIC -----

It is the object of this invention to solve the above mentioned problems with the prior art. This invention discloses a process for providing a self-aligned, LOD antiblooming structure whose antiblooming barrier height can be set by process (via implantation), and is relatively insensitive to process variations. An extra gate electrode to set the antiblooming barrier height is not required (as with some other disclosures), but may be provided so as to allow for electronic exposure control to use with FT image sensors. The antiblooming overflow channel length is determined photolithographically and is therefore, easily adjusted by layout. The process is simple and compatible with different types of gate dielectrics such as O (SiO.sub.2), ON (oxide nitride ), or ONO (oxide nitride oxide).





United States Patent  
Hawkins et al.

Patent Number: 5,516,716  
Date of Patent: May 14, 1996

(36) METHOD OF MAKING A CHARGE  
COUPLED DEVICE WITH EDGE ALIGNED  
DEPLETION LAYERS AND ELECTRODES

(37) INVENTOR: GORDON A. HAWKINS, MONTROSE, PA;  
L. LOUIS FALPHE, JR., NEW YORK

(38) Assignor: Eastman Kodak Company, Rochester,  
NY

(39) Appl. No.: 349,329

(40) Filed: Dec. 2, 1994

(41) Int. Cl. 6: H01L 31/02

(42) U.S. Cl.: 437/26; 437/28; 437/29

(43) Field of Search: 437/26, 33, 34,  
437/28, 437/29, 437/30, 437/31, 437/32

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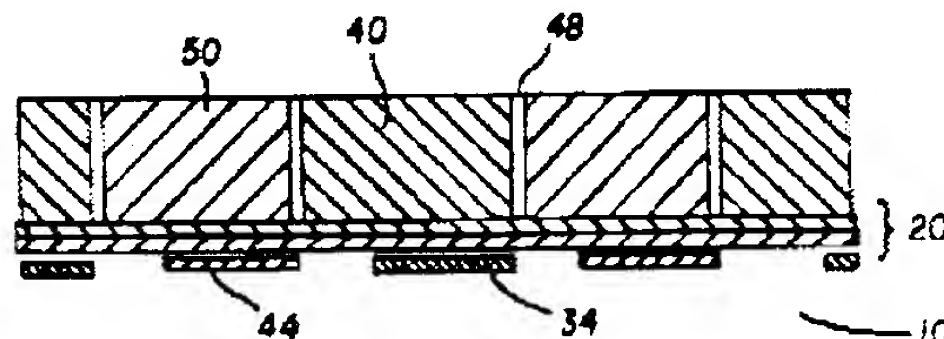
Boag, et al., Charge Transfer in the Presence of Potential Barriers, CDDP—The International Journal for Computer and Microelectronic in Electrical and Electronic Eng., vol. 28, No. 4, pp. 285-293, Dec. 1991.

Primary Examiner—Charles C. Smith  
Attorney, Agent, or Firm—Raymond L. O'Neil

## ABSTRACT

A fully self-aligned, charge coupled device (CCD) comprises a semiconductor substrate having implanted barrier under storage regions, an insulating dielectric layer disposed over the substrate, a first layer of closely spaced electrodes in self-alignment with at least one implant underneath the first electrodes, a second layer of closely spaced electrodes in self-alignment with the first electrodes and cells at least one implant underneath the second electrodes and in self-alignment with the first electrodes. The process for fabricating the fully self-aligned CCD comprises the steps of first forming upon the semiconductor substrate, a uniform thinning dielectric layer, then forming a sacrificial layer upon the dielectric layer, the sacrificial layer patterned by removal of selected portions of the layer, at least one edge of the patterned sacrificial layer serving as a mask for ion implantation into the semiconductor substrate, the mask optionally comprising also photoresist, then forming in only those regions in which the sacrificial layer was removed, a first gate electrode, then removing the sacrificial layer, thereby exposing the sidewalls of the closely spaced first gate electrodes, at least one of the sidewalls serving as a mask for a second ion implantation into the semiconductor substrate, the mask optionally comprising also photoresist, then forming a first oxide layer over the exposed surface of the first gate electrodes, then depositing and patterning a second gate electrode layer to form a second gate electrode disposed between portions of the first gate electrodes.

30 Claims, 9 Drawing Figures





**United States Patent**  
Hawkins et al.

Patent Number: 5,460,997  
Date of Patent: Oct. 24, 1998

**34** METHOD OF MAKING A CONDUCED  
PLANAR CHARGE COUPLED DEVICE  
WITH EDGE ALIGNED ELECTRODES  
AND INTERCONNECTED ELECTRODES

**35** Inventors: Gilbert A. Hawkins, Menden; Robert  
E. Menden, Princeton, both of N.Y.

**36** Assignee: Eastman Kodak Company, Rochester,  
N.Y.

**37** Appl. No. 09/04,904

**38** Filed: Jan. 22, 1998

**39** Int. Cl.<sup>6</sup> H01K 1/30

**40** U.S. Cl. 438/438; 438/438; 438/438

**41** Field of Search 438/438; 438/438; 438/438

**42** Primary Examiner: Charles C. Coughlin

**43** Attorney, Agent, or Firm: Raymond L. Owen

**44** U.S. Patent Documents

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